THEORY OF OPERATION

SECTION ORGANIZATION

This section of the manual contains a general summary of instrument functions followed by a detailed description of each major circuit. A basic block diagram, (Figure 9-4), and the schematic diagrams are located in the tabbed diagrams section at the back of this manual. They are used to show the interconnections between parts of the circuitry, to indicate circuit components, and to identify interrelationships with the front-panel controls.

The schematic diagram number associated with each description is identified in the text and is shown on the block diagram. For best understanding of the circuit being described, refer to the appropriate schematic diagram and the block diagram.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within the instrument. Functions and operation of the logic circuits are represented by logic symbology and terminology. Most logic functions are described using the positive-logic convention. Positive logic is a system where the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In this logic description, the TRUE state is HI, and the FALSE state is LO. The specific voltages which constitute a HI or a LO state vary between specific devices. For specific device characteristics, refer to the manufacturer's data book.

Linear Devices

The operation of individual linear integrated circuit devices in this section use waveforms or other techniques such as voltage measurement and simplified simplified diagrams to illustrate their circuit operation.

GENERAL DESCRIPTION

In the following overall functional description of the 2225 Oscilloscope, refer to the block diagram (Figure 9-4) located in the diagrams section of this manual. In Figure 9-4 the numbered diamond symbol in each major block refers to the appropriate schematic diagram number.

Vertical

Signals to be displayed on the crt (cathode-ray tube) are applied to either or both the CH 1 OR X and the CH 2 OR Y input connectors. The signals may be coupled to the attenuator either directly (DC) or through an input-coupling capacitor (AC). The inputs may also be disconnected, and the input to the attenuators grounded, by switching to the GND position of the input coupling switch. In the GND position, the ac-coupling capacitor is allowed to precharge to the dc level present at the input connector. This precharging prevents large trace shifts of the display when switching from GND to AC coupling. The Attenuators are switched by the front-panel VOLTS/DIV switches and scale the applied signal level to obtain the desired display amplitude.

The output signals from the Attenuators are applied to the Vertical Preamplifiers for amplification. The Channel 2 Preamplifier has additional circuitry, permitting the operator to invert the Channel 2 display on the cathode-ray tube (crt). Trigger pickoffs in each channel supply a trigger signal to the Trigger Amplifier when internal triggering is selected.

Input signals are selected for display by the Channel Switching circuit under control of the front-panel VERTICAL MODE switches. The output signal from

the Channel Switching circuit is applied to the Delay-line Driver stage. This stage converts a current input into a voltage output and provides an impedance match for the Delay Line. The Delay Line produces approximately 90 ns of delay in the vertical signal. This delay allows time for the Horizontal circuitry to start the sweep before the vertical signal is applied to the crt, so that the operator can see the signal that triggered the sweep.

Final amplification of the vertical signal is done by the Vertical Output Amplifier. This stage produces the signal levels that vertically deflect the crt electron beam. The upper frequency response of the Amplifier can be reduced by enabling the X10 Gain circuitry. For locating the position of off-screen displays, the dynamic range of the Amplifier can be limited with the Beam Find circuitry. This circuitry also intensifies the trace and limits horizontal deflection.

Triggering

The Trigger circuitry uses either the Internal Trigger signal obtained from the input signal(s), an External Trigger signal, or a Line Trigger signal derived from the ac-power-source to develop trigger signals for the Sweep Generator. The P-P Auto Trigger circuit sets the range of the Trigger Level to conform approximately to the peak-to-peak amplitude of the selected trigger signal when either Auto or TV Field Trigger mode is selected. This allows triggering on most signals without needing to adjust the TRIGGER LEVEL control. In Norm mode, the TRIGGER LEVEL control must be adjusted to the signal level before a sweep will be triggered.

The triggering circuitry contains the TV Field Sync circuit. This circuit provides stable triggering on television vertical-sync pulses when in the TV Field triggering mode. TV Line triggering is possible using P-P AUTO trigger mode.

Sweep

The Sweep Logic circuit controls the sweep generation and Z-Axis unblanking for the Sweep display. When the TRIGGER Mode switches are set to either P-P AUTO or TV FIELD and no trigger signal is present, the Auto Baseline circuit causes the Sweep Logic circuit to produce a sweep for reference purposes. In the NORM setting, the Auto Baseline circuit is disabled and sweeps are not generated until a trigger event occurs. This is useful for triggering on low-repetition rate signals. The SGL SWP (single sweep) trigger mode allows only one sweep to be generated after being reset. Following the single sweep, the Trigger circuit is disabled until the SGL SWP RESET button is pressed again.

The Sweep Logic circuit controls the operation of the Miller Sweep Generator circuit. The Sweep circuit produces a linear sweep with a ramp time that is controlled by the SEC/DIV switch setting. The sweep signal is applied to the Horizontal Preamplifier for initial amplification and then to the Horizontal Output Amplifier to drive the crt horizontal deflection plates.

Horizontal

The Horizontal Preamplifier gain is increased by a factor of 5, 10, or 50 when the Horizontal MAG control is used. Horizontal positioning of the display is accomplished in the Horizontal Preamplifier circuit.

In the X-Y mode of operation, the Channel 1 signal from the internal Trigger circuitry passes through the X-Y Amplifier to the Horizontal Preamplifier. In this operating mode, the Channel 1 Internal Trigger signal supplies the horizontal deflection to the crt, and the Miller Sweep circuit is disabled to inhibit sweep generation.

Z-Axis

The Z-Axis drive from the Sweep Logic circuit is applied to the Z-Axis Amplifier. The output signal from the Z-Axis Amplifier circuit sets the crt intensity. When using Chop Vertical mode, a blanking signal from the Chop Oscillator circuit blanks the crt display while switching between the vertical channels.

The DC Restorer circuit applies the output voltage of the Z-Axis Amplifier between the cathode and grid of the crt. High dc potentials on these elements prohibit direct coupling to the crt.

Power Supply

The Power Supply provides the necessary operating voltages for the instrument. Operating potentials are obtained from a circuit consisting of the Power Transformer, Pre-regulator, Inverter and multi-winding transformer. The voltage produced by the Power Transformer output winding, after rectification, provides 45 Vdc minimum to the 40-kHz Preregulator circuit, which in turn, supplies a nominal 38 Vdc to the 20 kHz Inverter stage. A High Voltage Multiplier circuit produces the accelerating, focus, and cathode potentials used by the crt.

Probe Adjust

A front-panel PROBE ADJUST output is provided for use in adjusting probe compensation. The voltage at the PROBE ADJUST terminal is a negative-going square wave that has a peak-to-peak amplitude of approximately 0.5 V with a repetition rate of approximately 1 kHz.

DETAILED CIRCUIT DESCRIPTION

VERTICAL

Attenuators

The Channel 1 and Channel 2 Attenuator circuits, shown on diagram 1, are identical with the exception of the additional Invert circuitry in the Channel 2 Paraphase Amplifier. Therefore, only the Channel 1 Attenuator is described, with the Invert circuitry of Channel 2 discussed separately.

The Attenuator circuit (see Figure 3-1) provides control of the input coupling, the vertical deflection factor, and the variable volts/division gain. Vertical input signals for display on the crt may be connected to either or both the CH 1 OR X and the CH 2 OR Y input connectors. In the X-Y mode of operation, the signal applied to the CH 1 OR X connector provides horizontal (X-axis) deflection for the display, and the signal applied to the CH 2 OR Y connector provides the vertical (Y-axis) deflection for the display.

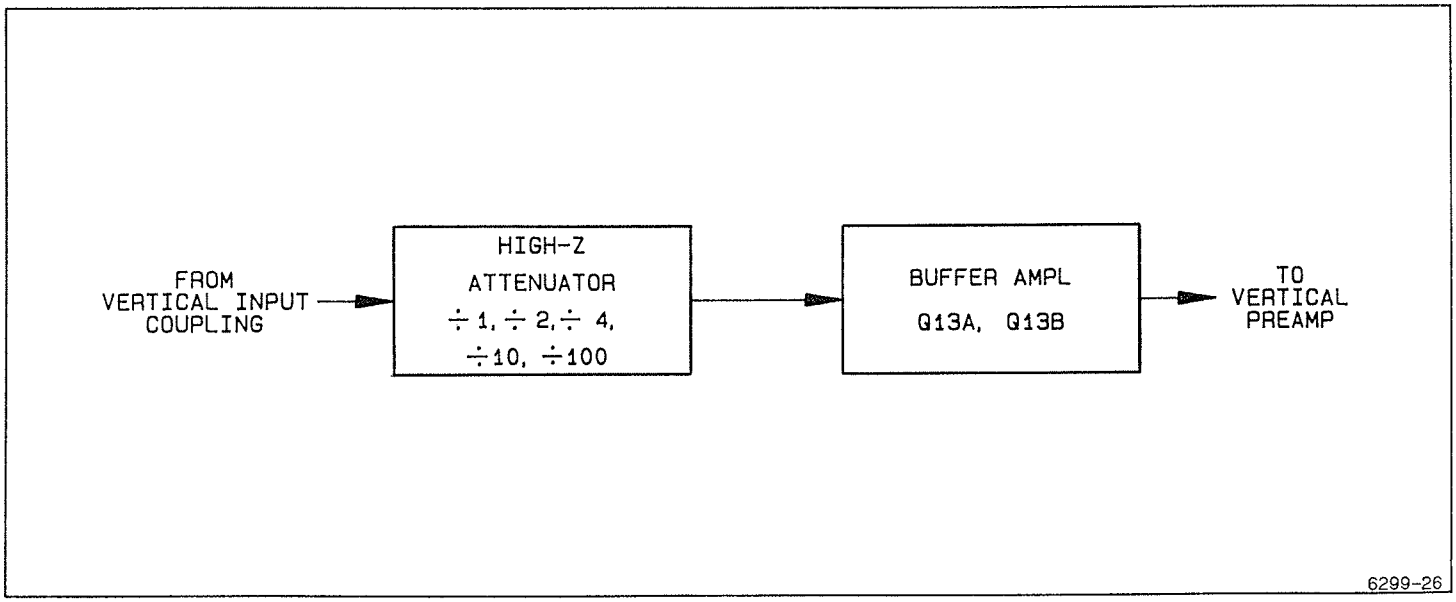

Figure 3-1. Block diagram of the Channel 1 Attenuator circuit.

Input Coupling (AC-GND-DC)

A signal from the CH 1 OR X input connector may be ac or dc coupled to the High-Impedance Attenuator circuit or disconnected completely by the Input Coupling Switch. Signals from the CH 1 OR X input connector are routed through resistor R1 to Input Coupling switch S101. When S101 is set for dc coupling, the Channel 1 signal goes directly to the input of the High-Impedance Attenuator stage. When ac coupled, the input signal passes through dc-blocking capacitor C2. The blocking capacitor stops the dc component of the input signal from reaching the Attenuator circuit. When switched into the signal path, attenuator AT1 attenuates the input signal by factors of 100, 10, 4, or 2. When S101 is set to GND, the direct signal path is opened, and the input of the attenuator is connected to ground. This provides a ground reference without the need to remove the applied signal from the input connector. The coupling capacitor precharges through R4 to prevent large trace shifts when switching from GND to AC.

Input Attenuator

The effective overall deflection factor of each vertical channel is determined by the setting of the Channel VOLTS/DIV switch. The basic deflection factor of the Vertical system is 5 mV/DIV. For VOLT/DIV switch settings above 5 mV/DIV, frequency compensated voltage dividers (attenuators) are switched into the circuit. Each channel has 2X, 4X, 10X, and 100X attenuators that are selected in various combinations to produce the indicated deflection factor. Each attenuator contains an adjustable series capacitor to provide correct attenuation at high frequencies and an adjustable shunt capacitor to provide correct input capacitance.

Source Follower

The Channel 1 signal from the input attenuator is connected to source follower Q13A via R6 and C6. Resistor R5 provides the input resistance. FET Q13B is a constant current source for Q13A. Transistors Q13A and Q13B provide a high input impedance for the attenuator stage and the output drive current needed for Paraphase Amplifier U30 (the first stage of amplification).

In the event that excessive high-amplitude signals are applied to source follower Q13A, the signal will be limited by CR7 and the gate-source junction of Q13A. If an excessive negative-going signal causes CR7 to become forward biased, Q13A gate is clamped to approximately -9.3 V. An excessive positive-going signal will forward bias the gate-source junction of Q13A. As soon as gate current flows, the gate voltage will stop increasing. Gate current is limited by the high resistance of R6.

Paraphase Amplifier

Paraphase Amplifier U30 converts the single-ended signal from Q13 into a differential signal for the Vertical Preamplifier. The signal from Q13B pin 2 goes to the base of one transistor in U30. The other input transistor in U30 is biased by the divider network formed by R30, R31, R32, and R33. Emitter current for the two input transistors is supplied by R22 and R23. Resistor R29 sets the gain for the stage. The network formed by C8 and R9 reduce the substrate capacitance of Q13 at high frequencies. R8 biases the diode substrate of Q13 off. The collector current of the two input transistors serves as emitter current for the differential output transistor pairs. Base bias voltages for the output pairs are developed by the divider network formed by R39, R41, R42, and Variable VOLTS/DIV potentiometer R43. The transistors of U30 have matched characteristics, so the ratio of currents in the two transistors, U83C and U83D, connected as diodes, determines the current ratios in the output transistor pairs of U30.

As Variable VOLTS/DIV potentiometer R43 is rotated from calibrated to uncalibrated, the conduction level of the transistors connected to R35 increases. Since the transistor pairs are cross connected, the increased conduction in one pair of transistors subtracts from the output current produced by the transistor pair connected to R38, and the overall gain of the amplifier decreases. Balance potentiometer R33 is adjusted to balance the amplifier for minimal dc trace shift as the CH 1 Variable VOLTS/DIV control is rotated.

Incorporated in the Channel 2 Paraphase Amplifier is circuitry that allows the user to invert the polarity of the Channel 2 signal. When CH 2 INVERT switch S90 is selected for NORM, the transistor pairs in U80 are biased as they are in U30, and the CH 2 trace is not inverted. For the CH 2 INVERT position of S90, connections to the bases of the output transistor pairs are reversed, reversing the polarity of the output signal to produce an inverted Channel 2 trace. Invert Balance potentiometer R83 is adjusted

for minimal dc trace shift in CH 2 INVERT when rotating CH 2 Variable VOLTS/DIV. Balance Potentiometer R84 is switched in with R83 when in NORM; it is adjusted for minimal dc trace shift when rotating CH 2 Variable VOLTS/DIV.

Vertical Preamplifiers

The Channel 1 and Channel 2 Vertical Preamplifiers, shown on diagram 2, are identical in operation. Operation of the Channel 1 amplifier is described. Differential signal current from the Paraphase Amplifier is amplified to produce drive current for the Delay Line Driver. Internal trigger signals for the Trigger circuitry are picked off prior to the Vertical Preamplifier. The Channel Switch circuitry controls channel selection for the crt display.

Common-base transistors Q102 and Q103, which complete the Paraphase Amplifier portion of the circuitry shown on diagram 1, convert differential current from the Paraphase Amplifier into level-shifted voltages that drive the bases of the input transistors of Vertical Preamplifier U130 and the Internal Trigger circuitry.

Common-mode components CR104, CR105, R104, and R105 provide X1 gain. X10 gain is selected by switching in CR111, CR112, R107, R110, R111, R112, and R128. X10 gain is adjusted by R112, and X10 balance is set by R107. C110 limits the bandwidth in X10 mode to about 5.2 MHz to 7.8 MHz.

Emitter current for the input transistors of U130 is supplied by Q114 and Q115. The base bias voltage to Q114 and Q115 is unbalanced through potentiometer R123 (the CH 1 POSITION control) to produce vertical positioning of the Channel 1 trace. The collector current of each input transistor of U130 is the emitter current for two of the differential output transistors. One of the collectors of each output pair is grounded, and the other provides output drive to the Delay Line Driver. The base bias voltages of the transistors with grounded collectors are held at ground potential by R136. The base voltages of the other transistors are controlled by the Channel Switch circuitry.

When Channel 1 is selected to drive the Delay Line Driver, the Q output (pin 9) of U540A is HI. The transistors with the ungrounded collectors are then forward-biased, and the Channel 1 signal is conducted through to the Delay Line Driver. If Channel 1 is not selected, then the Q output of U540A is LO. The transistors with the ungrounded collectors are then reverse-biased, and the output signals will be conducted to ground by the other transistor pair. The gain of the Preamplifier is set by adjusting R145 to control the signal current that is shunted between the two differential outputs.

Channel Switch Logic

The Channel Switch circuitry, shown on diagram 2, utilizes the front-panel VerticaL MODE switches to select the crt display format. See Figure 3-2 for a block diagram of the circuit.

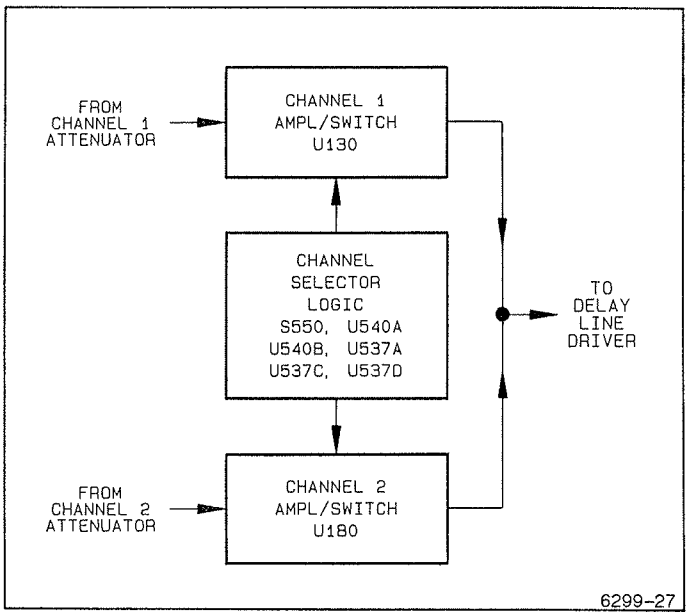

Figure 3-2. Block diagram of the Channel Switching circuit.

When any display mode other than X-Y is selected, the XY line connected to S550 is at ground potential. Vertical MODE switches S545 and S550 control the connection between the XY control line and the SET and RESET inputs of flip-flop U540A (SET and RESET are active LO) to obtain the various display formats described below.

CHANNEL 1 DISPLAY ONLY. The CH 1 position of S550 grounds the SET input of U540A while the RESET input is held HI by pull-up resistor R539. This sets U540A and produces a HI and a LO on the Q and $\overline{Q}$ outputs respectively, and the Channel 1 Preamplifier signal then drives the Delay Line Driver (as described in the Vertical Preamplifier section). The Channel 2 Preamplifier will be disabled.

CHANNEL 2 DISPLAY ONLY. The CH 2 position of S550 holds the RESET input of U540A LO through CR538, and the SET input is held HI by pull-up resistor R538. This resets U540A, making the Q output of U540A LO and the $\overline{Q}$ output HI. The Channel 2 Preamplifier signal is then enabled to drive the Delay Line Driver, while the CH 1 Preamplifier is disabled.

To display the ADD, ALT, or CHOP formats, S550 must be in the BOTH position to ground the A, C, and F pins of S545.

ADD DISPLAY. In the ADD position of S545, both the SET and RESET inputs of U540A are held LO by CR534 and CR537. This forces the Q and $\overline{Q}$ outputs of U540A both HI, and signal currents from the Channel 1 and Channel 2 Preamplifiers add together to drive the Delay Line Driver.

CHOP DISPLAY. In the CHOP position, the $\overline{\text{CHOP ENABLE}}$ line is held LO, keeping the Q output of flip-flop U540B HI. This enables CHOP multivibrator U537D to begin switching. The switching rate is determined primarily by the component values of R544, R545, and C545. The output of U537C (the inverted output of the multivibrator circuit) supplies the CHOP clock to flip-flop U540A via U537A. The output of U537C also drives U537B, the CHOP Blanking Pulse Generator.

Coupling capacitor C547 and resistors R547 and R548 form a differentiating circuit that produces positive-going and negative-going short duration pulses. These pulses are inverted by U537B to generate the Chop Blank signal to the Z-Axis Amplifier. The pulses blank the crt during CHOP switching times.

The Alt Sync signal applied to one input of U537A is HI except during Holdoff. This allows the output of U537C to be inverted by U537A which drives the clock input of U540A. Since the $\overline{Q}$ output of U540A is connected back to the D input, and both the SET and RESET inputs are HI (unasserted), the outputs of U540A toggle (change states) with each clock input. The Delay Line Driver is then driven alternately from the Channel 1 and Channel 2 Preamplifiers at the CHOP rate.

ALTERNATE DISPLAY. In ALT, the $\overline{\text{CHOP ENABLE}}$ line is held HI, disabling CHOP multivibrator U537D. The output of U537C will be HI and the CHOP BLANK signal from U537B will be LO. Input signals to U537A are the HI from U537C and the ALT SYNC signal from the Holdoff circuitry in the Sweep Generator. The output of U537A will then be the inverted ALT SYNC signal that clocks Channel Select flip-flop U540A. This causes the outputs of U540A to toggle at the end of each sweep so that the Channel 1 and Channel 2 Preamplifiers alternately drive the Delay Line Driver.

Delay Line Driver

The Delay Line Driver converts the signal current from the Vertical Preamplifiers into a signal voltage for input into the Delay Line. Transistors Q202, Q203, Q206, and Q207 form a differential shunt feedback amplifier with the gain controlled by R216 and R217. Common-mode dc stabilization of the Delay Line Drive Amplifier is provided by U225. Should the voltage at the junction of R222 and R223 deviate from zero, U225 will sink or source base current to Q202 and Q203 through R202 and R203. This will return the outputs of the Delay Line Driver to an average dc value of zero volts. Delay Line DL224 provides a vertical signal delay of approximately 90 ns so that the Sweep Generator has sufficient time to produce a sweep before the vertical signal that triggered the sweep reaches the vertical deflection plates.

Vertical Output Amplifier

The Vertical Output Amplifier drives the vertical deflection plates of the crt. Signals from the Delay Line go to a differential amplifier formed by Q230 and Q231 with low- and high-frequency compensation provided by the RC networks between the emitters. Thermal compensation is provided by thermistor RT236, and overall circuit gain is set by R233. The output stage of the amplifier is two, compound-shunt transistor pairs, Q254-Q256 and Q255-Q257, that convert the collector currents of Q230 and Q231 to proportional output voltages. Resistors R256 and R257 serve as feedback elements. High-frequency compensation is provided by C256 and C257.

Vertical Beam Find

Beam Find is used to reduce the vertical trace deflection to within the graticule area for locating off-screen and over-scanned traces. BEAM FIND switch S390 adjusts the Delay Line Driver amplifier biasing to limit the voltage swing at the crt plates. When S390 (diagram 6) is in the normal position (not pressed), the BEAM FIND voltage level on R226 is about 0.4 V. When the BEAM FIND switch is pressed, the voltage level on R226 goes to about -8.6 V. This level forces the output of U225 LO and biases Q202 and Q203 such that the amplifier dynamic range is limited.

Alternate Sweep Separation

The circuit consisting of Q283, Q284, Q285, and associated components provides a means of vertically positioning the Alternate (Magnified) sweep, with respect to the X1 mode trace during Alternate Horizontal Mode displays. During the Alternate (Magnified) sweep interval, the $\overline{\text{SEP}}$ signal from the Alternate Display switching circuit is LO, and Q283 is biased off. This allows TRACE SEP potentiometer R280 to affect the bias on one side of a differential current source composed of Q284 and Q285. The potentiometer supplies a dc offset current to the Vertical Output Amplifier that changes the position of the Alternate trace on the screen.

During the X1 Mode sweep interval the $\overline{\text{SEP}}$ signal is HI (unasserted), and Q283 is biased on. The base voltages of Q284 and Q285 are then the same, and equal current is supplied to both sides of the amplifier so that no offset of the trace occurs.

TRIGGER

The Trigger Amplifier, shown on diagram 3, provides signals to the Trigger Generator from either the Vertical Preamplifiers, the EXT INPUT connector, or the power line. The SOURCE switch selects between Channel 1, Channel 2, line, or external trigger sources. The COUPLING switch selects AC, DC, LF REJECT, or HF REJECT trigger-signal coupling.

Internal Trigger

Signals from the Vertical Preamplifiers drive the CH 1 and CH 2 Internal Trigger Amplifier with channel selection determined by the Vertical and Horizontal MODE switches. Trigger pickoff from the Preamplifiers is accomplished by U315B and U315C for Channel 1 and U325A and U325B for Channel 2. The circuitry associated with Channel 2 is the same as Channel 1 except that it does not have a trigger-offset adjustment.

Differential vertical signals from the Channel 1 Preamplifier go to U315B and U315C. These emitter-follower transistors each drive one input transistor in U335. The collectors of the U335 input transistors in turn supply emitter current to two pairs of current-steering transistors. The compensation and biasing network connected between the emitters of the input transistors in U335 is fixed for Channel 2 but not for Channel 1. Potentiometer R338 in the emitter circuit adjusts the bias levels of the two input transistors to match the dc offsets of the Channel 1 and Channel 2 Trigger Amplifiers.

One transistor in each side of the output differential amplifier pairs of U335 has its base bias set to zero volts. The bias voltage of the other transistor in each pair is controlled by the CH 1 TRIG signal from the Trigger Switch circuitry. When the CH 1 TRIG signal is LO, the transistors in each output pair with the collectors connected together are biased on, and the other transistors in the output pairs are off. The collector signal currents of the conducting transistors are equal in magnitude but of opposite polarity, so signal cancellation occurs. When the CH 1 TRIG signal is HI, the other transistors in each pair are biased on, and a differential signal is developed across output load resistors R339 and R340 to drive the Internal Trigger Amplifier.

Internal Trigger Amplifier

Internal trigger channels are chosen by the SOURCE switch being set to CH 1, VERT MODE, or CH 2. The logic function required to generate CH 1 TRIG and CH 2 TRIG is performed by U300, U304, CR300, CR301, and CR302. External Trigger is selected by the SOURCE switches being set to EXT, and EXT=Z or EXT or EXT/10. Line Trigger is selected by the SOURCE switches being set to EXT and LINE.

CHANNEL 1. When the Trigger SOURCE is set to CH 1, Channel 1 is the trigger source whether displayed or not. The Channel 1 signal is also the trigger source under other settings of the Trigger SOURCE and Vertical MODE switches that call for the Channel 1 signal to be displayed. Those conditions are:

Trigger SOURCE set to VERT MODE and the Vertical MODE is set to CH 1, or

Trigger SOURCE set to VERT MODE and the Vertical MODE is set to BOTH and ALT.

CHANNEL 2. When the Trigger SOURCE is set to CH 2, then Channel 2 provides the trigger signal whether Channel 2 is displayed or not. As with Channel 1, other Trigger SOURCE and Vertical MODE settings will call up the Channel 2 as the trigger signal when Channel 2 is displayed. Those conditions are:

Trigger SOURCE set to VERT MODE and the Vertical MODE is set to CH 2, or

Trigger SOURCE set to VERT MODE and the Vertical MODE is set to BOTH and ALT.

VERT MODE. When the SOURCE switch is set to VERT MODE the trigger source selection is determined by the Vertical MODE switch. Vertical MODEs of CH 1, CH 2, and BOTH in ALT are described above. Vertical MODEs of BOTH in ADD or CHOP result in the trigger source being the arithmetic sum of the Channel 1 and Channel 2 input signals.

EXT. When the SOURCE switches are set to EXT, and either EXT=Z or EXT, the trigger source is the signal applied to the EXT INPUT OR Z connector. With EXT and EXT/10 selected, the trigger signal is as above but attenuated by a factor of 10. With EXT and LINE selected, the line-frequency signal, generated in the power supply, is passed to the External Trigger Input Amplifier (shown on diagram 6). In each case, the buffer consisting of Q370A and Q370B, drives differential amplifier U340. This amplifier has the same form as the CH 1 and CH 2 preamplifiers. External offset adjustment is provided by R360. The LO logic signal generated by U308B, $\overline{\text{EXTEN}}$, switches on the external trigger path.

Trigger Amplifier

The Trigger Amplifier converts the differential signals from the vertical and external preamplifiers into a single-ended analog trigger signal that drives the X-Axis amplifier (for X-Y Mode displays) and the Trigger Generator.

Transistors Q363 and Q365 act as a cascade stage to add the signals passed by the preamplifiers to the offset current provided by the coupling control amplifiers on diagram 3. The resulting differential output drives the differential pair Q366 and Q367. The collector load of transistor Q367 is R388. That load is driven via cascode transistor Q368 and "diode-connected" transistor U380D. Transistor Q366 drives current mirror U370D and U370B. Diode CR370 ensures that the collector-base voltage of U370D is not too low, and CR369 compensates for U370C, to equalize the collector potentials of U370B and U370D.

The collector current of U370C is the output of the current mirror and is equal to the collector current of Q366. R388 passes a current equal to the difference in the collectors of Q366 and Q367 (the trigger signal). Transistor U380C acts as an impedance buffer, whose voltage drop is compensated by U380D. The output from the emitter of U380C is the analog trigger signal. In X-Y mode, U380B is biased off, allowing the trigger signal to be passed to the X-Axis Amplifier. U380E is switched off when HF REJECT is selected. This allows C372 to be switched in by U380A, thereby shunting signals of frequencies about 30 kHz and above.

Peak Rectifiers

The analog trigger signal is passed to the positive and negative Peak Rectifier circuits, The Peak Rectifiers generate voltages equal to the positive and negative peaks of the analog trigger waveform in P-P AUTO and TV FIELD modes. In NORM and SGL SWP modes, the Peak Rectifier outputs assume a voltage of about the full peak-to-peak limits of the trigger signal.

The analog trigger signal is applied to the bases of U415B and U435A. In P-P AUTO, C418 charges to the positive peak of the analog trigger signal less the U415B base-emitter drop. The base-emitter drop of U415D compensates so that the output of U425B is equal to the positive peak of the analog trigger signal. In NORM Trigger mode, the base drive to U415A rises to about +3 V, which drives the output of U425A to this level.

In P-P AUTO, C431 charges to the negative peak of the analog trigger signal, and Q435 will only switch on if the base drive to U435 is less than that of U435B. If Q435 switches on, then C431 will discharge to a more negative voltage so the output of U425A will track the negative peak of the analog trigger signal. In NORM mode, U415E switches on, and C431 charges to about -3 V via CR431. Trigger LEVEL control R426 selects a trigger level voltage between the peak rectifier outputs to give trigger operation over a sufficient dynamic range.

Coupling Circuit

The Trigger Amplifier is optimized for bandwidth, not dynamic range. A current is added to the summing stage of Q363 and Q365 (via R397 and R398) to shift the desired switching point on the analog trigger signal to the threshold of the Schmitt Trigger circuit (fixed at zero volts). The selection of current drivers to feed the Trigger Amplifier is achieved by emitter switching of differential pairs U445C and U445D, U445A and U445B, and U435C and U435D. In NORMAL DC coupling, a fixed current proportional to the voltage on the LEVEL control is passed to the summing stage by U445C and U445D. This is enabled by logic signal DC from U308A being HI to bias on Q420.

In NORMAL AC coupling, the dc component of the analog trigger signal is extracted by a low-pass filter circuit R470, C471, C472, and U415C. The dc component is added to the LEVEL voltage, and the result is fed into amplifier U450A. The output of U450A controls differential pair U435C and U435D and completes the feedback loop that adjusts the offset current so that the input of U450A is held at zero volts. This forces the DC component of the analog trigger signal to be equal and opposite to the LEVEL voltage, giving AC coupling with DC shift. LF REJECT operates in exactly the same way, except that the time constant of the low-pass filter is changed by switching off U415C, allowing C473 to dominate the circuit. P-P AUTO operates by establishing a feedback loop with U450B to hold the voltage on LEVEL at zero. Note that P-P AUTO does not distinguish between DC and AC coupling.

Trigger Level Comparator

The Trigger Level Comparator compares the level of trigger signals selected by the Trigger SOURCE switch to a zero voltage level. Positive- or negative-slope triggering is selected by the front-panel Trigger SLOPE switch.

The analog trigger signal drives the base of U460B. The transistors of U460 form a differential amplifier. With the input to U460E grounded, it is effectively a "single-ended" to differential amplifier. The cross-coupled collector outputs can reverse the direction of the signal fed to the succeeding stage depending on the selection by the SLOPE control.

Schmitt Trigger and TV Trigger Circuit

This circuitry generates a signal that drives the Trigger Logic as a function of the Trigger Level Comparator output signal and the Trigger MODE switches.

The output signals from the Trigger Level Comparator drive Q400 and Q401. These transistors are configured as a current mirror that converts the differential output to a single-ended current to drive amplifier U480C. Slope Balance potentiometer R481 corrects for dc offsets between positive and negative slopes. Shunt feedback amplifier U480C converts a current input to a voltage output to drive the input of the Schmitt Trigger, U480D, through R485. Positive feedback for the Schmitt Trigger is provided by Trigger Sensitivity potentiometer R489, and C489 reduces trigger jitter by increasing positive feedback at higher frequencies. The setting of R489 determines the circuit hysteresis.

When TV FIELD is not selected, the $\overline{\text{TVF}}$ signal connected to R487 is HI (unasserted). Transistors Q488 and Q489 are biased off, and a LO is placed on one input of U480A by R492-R493. This LO input will cause U480A to invert the output from U480D. With Q489 off, a LO will be placed on one input of U480B by R495, and U480B will also act as an inverter. The Trigger signal at the output of U480B is therefore the same as the input signal to U480A.

When TV FIELD is selected, the $\overline{\text{TVF}}$ line is LO (asserted). The outputs of U480D will determine the conduction states of Q488 and Q489, and the input of U480A connected to R492 will be HI. The output of U480A will be LO, and U480B will invert the signal at its other input. Signals at the collector of Q489 are filtered by C495, R495 and C496 to reject TV Video information and average the TV horizontal-sync pulses. Setting the trigger-level threshold near the center of the horizontal-sync-pulse swing establishes the untriggered level. When the TV vertical-sync block occurs, the output of the filter

applied to U480B pin 7 rises to a level that will cause the Trigger output gate U480B pin 3 to switch. Precise TV field synchronization is obtained as a result of this filtering action. The Trigger signal output will be the inverse of the filtered signal appearing at U480B pin 7.

SWEEP AND SWEEP GENERATOR LOGIC

The Sweep Logic circuitry and the Sweep Generator circuitry, shown on diagrams 4 and 5 respectively, produce a linear voltage ramp that drives the Horizontal Preamplifier. The Sweep Logic circuit also produces signals that are used to generate correct timing of the crt unblanking and intensity levels used for viewing the display. See Figure 3-3 for the block diagram of the Sweep Generator and Logic circuitry.

Miller Sweep Generator

The Miller Sweep Generator (diagram 5) produces a linear voltage ramp that drives the Horizontal Amplifier. It produces the ramp voltage by maintaining a constant current through timing capacitors, causing a linear voltage rise across them as they charge.

Field-effect transistors Q704A and Q704B are matched devices with Q704B acting as the current source for Q704A. Since the gate and source of Q704B are connected together, the source current available to Q704A is just enough so that there is no voltage drop across the gate-source junction of Q704A.

When the sweep is not running, Q701 is biased on, holding the selected timing capacitors in a discharged state. The low impedance of Q701 in the feedback path holds the Miller Sweep output near ground potential. The voltage across Q701, in addition to the base-emitter voltage of Q706, prevents Q706 from becoming saturated.

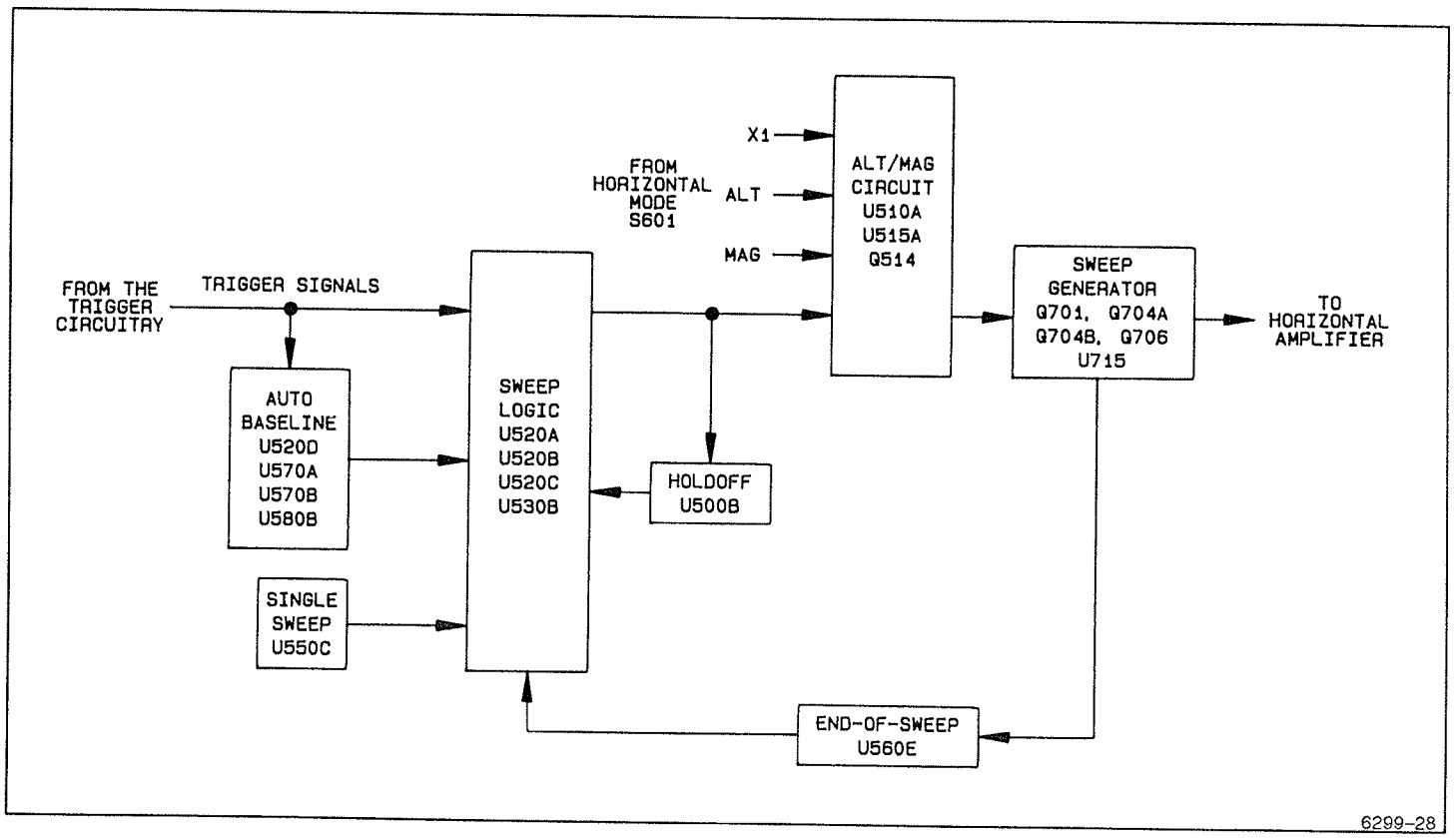

Figure 3-3. Block diagram of the Sweep Generator and Logic circuit.

The sweep ramp is initiated when Q536 (diagram 4) is biased off. The $\overline{\text{GATE}}$ signal going to the base of Q701 from the Sweep Logic circuit turns Q701 off. The timing capacitors then begin charging at a rate set by timing resistors R701, R702, and the position of the SEC/DIV switch S701. One end of timing resistor R701 is connected to the wiper of R721, and the other end is connected to the input of the Miller integrator. Due to feedback from the circuit output through the timing capacitors, the integrator input voltage at the gate of Q704A remains fixed and sets a constant voltage across the timing resistors. This constant voltage produces a constant charging current through the timing capacitors, which results in a linearly increasing voltage ramp at the output of the Miller Sweep circuit.

When the ramp reaches approximately 12 V, the Sweep Logic circuitry will initiate the holdoff period during which Q701 is turned on and the Sweep Generator is reset. This holdoff period is necessary so that the timing capacitors can be fully discharged before another sweep starts. Capacitors C704 and C703 are always in the charging circuit and are used for high sweep speeds. Capacitors C701 and C702 are used for medium sweep speeds; C701 alone is used for slow sweep speeds.

The SEC/DIV Variable circuitry utilizes an operational amplifier to maintain a constant reference voltage at one end of R721 independent of the circuit load. The voltage applied to the timing resistors varies with the setting of R721, the SEC/DIV Variable control. A fixed dc voltage is applied to the noninverting input of the operational amplifier, and feedback resistors R717 and R718 establish double that voltage at the anode of VR719. Resistor R722 is used to adjust the reference voltage when in the 0.5 ms to 10 µs SEC/DIV ranges to correct for mismatch between timing capacitors C701 and C702.

Sweep Logic

The purpose of the Sweep Logic circuit (diagram 4) is to control the sweep start dependent upon the trigger signal and Trigger MODE setting. It also provides the signal for Alternate Channel Switching and Alternate Magnification.

NORM. When NORM trigger is selected, the circuit is ready to start the sweep in response to a trigger signal. U530B has a LO on the SET, RESET, and D input. A trigger pulse received at the CLOCK pin of U530B will clock the LO on the D input to the Q output and enable the sweep to start. The output of the sweep generator is fed back via W701-3 into the potential divider R501 and R502. This divider is arranged so that when the ramp voltage reaches approximately 12 V, U560E is turned on, producing a LO on the input of inverter U520A. The signal from U520B is inverted by U520C to give an overall OR function which is fed to the SET input of U530B. This overrides the CLOCK input and puts a HI on the Q output, resetting the sweep. The sweep reset is also fed to the input of monostable multivibrator U500B, which gives a holdoff time dependent upon the holdoff capacitor selected and the variable holdoff resistor chain. The holdoff pulse from the monostable maintains the HI on the SET input of U530B until the end of the holdoff period. At that time the SET is driven LO, allowing the next trigger pulse to start the sweep.

P-P AUTO. In the P-P AUTO mode, the sweep will free-run in the absence of a trigger signal. Should there be more than 50 ms between trigger pulses, the Auto Baseline circuit, consisting of U580B, U520D, U570A, and U570B, will initiate a sweep. The circuit of U580B is a 20-Hz clock pulse generator. The 20-Hz clock signal is passed through Schmitt trigger U520D to provide a fast rise time. This is to ensure that U570A pin D and U570B pin D switch at the same time.

With no trigger signal, the first clock pulse from U580B resets U570A, putting a HI on the D of U570B. This will then be clocked (giving a LO on TRIGGERED) when the next 50-ms pulse arrives. If the end of sweep has occurred and the holdoff period has elapsed, then the output of U520C will be LO. Because TRIGGERED and P-P AUTO are both LO, the output of U550D will put a LO on one input of U550B. As the other input is also LO, the output of U550B will put a HI on the RESET pin of U530B. That resets the flip-flop, placing a HI on the base of Q536 that turns it off and forces $\overline{\text{GATE}}$ LO at the collector of Q536 to initiate a sweep.

If a trigger occurs, the HI on the D pin of U570A is passed to the Q of U570A, to reset U570B, and put a HI on the TRIGGERED line. The output of U550B will then be LO, allowing U530B to respond to the next trigger signal. When the TRIGGERED line is HI the TRIG'D/READY light is turned on via U550A.

SINGLE SWEEP. When the SGL SWP MODE is selected, the $\overline{\text{SINGLE SWEEP}}$ line is LO, holding the D input of U570A LO. This effectively disables the

Auto Baseline Generator and also puts a LO on the TRIGGERED line. At the end of a sweep, the holdoff pulse is latched by U530A via U520B and U550C, and the D input of U530B is driven HI. Thus the sweep will not start on receipt of a trigger. This condition is cleared by a pulse from single-shot monostable U500A, that clocks the LO on the D input of U530A to the Q output, allowing the next trigger to initiate a sweep. U500A is used as a switch debounce circuit. Timing components R506 and C506 are chosen to give a pulse width of about 30 ns, a pulse that is shorter than the fastest sweep speed. U500A also sets U510B, turning the TRIG'D light on via U550A. When the holdoff period is initiated (and U500A has timed out), U500B will clock a LO back onto the Q output of U510B, allowing the TRIG'D light to be turned off.

Alternate Magnification

The ALT Magnification mode is controlled by S601. In the X1 mode, $\overline{X1}$ is LO to set flip-flop U510A. The Q output of U510A ($\overline{SEP}$) is therefore HI. This HI is inverted and level shifted by Q514 to drive the MAG line LO to the Horizontal Amplifier. In MAG mode, the $\overline{MAG}$ line from S601 is LO, and flip-flop U510A is reset. $\overline{SEP}$ is therefore LO, driving the MAG line HI to the Horizontal Amplifier. The $\overline{SEP}$ signal line controls the trace separation circuitry in the Vertical Amplifier. In the ALT mode, U510A divides the ALT SYN signal by two so that on every other sweep the $\overline{SEP}$ and MAG lines are TRUE.

Alternate Channel Switching

The ALT SYNC signal is provided for the channel switching circuit so that when ALT Vertical MODE is selected, channel switching will be synchronized with the timebase. When ALT MAG is not selected, the alternate switching pulse (ALT SYNC from U515A, pin 3) is supplied at the end of each sweep to the channel switching logic circuit. When ALT MAG is selected, flip-flop U510A divides ALT SYN by two so that the ALT SYNC channel switching pulse is supplied after each second sweep. This produces the following sequence of displays:

CH1 MAG
CH1 X1
CH2 MAG
CH2 X1

When BEAM FIND switch S390 (diagram 6) is pressed, the emitter of Q776 (diagram 5) goes LO to about -8V. That voltage is applied to R510 and C511. Diode CR511 clamps the cathode of CR510 to about -0.6V, so about 0 V is applied to the SET pin of U510A to set that flip-flop. The Q output of U510A is therefore HI, disabling the sweep separation and MAG circuits.

HORIZONTAL

The Horizontal Amplifier circuit, shown on diagram 5, provides the signals that drive the horizontal deflection plates of the crt. Signals applied to the Horizontal Preamplifier may come from either the Miller Sweep Generator (for sweep deflection) or from the X-Y Amplifier (when X-Y display mode is selected). See Figure 3-4 for the block diagram of the Horizontal Amplifier.

The Horizontal POSITION control, X5, X10, X50 Magnifier circuitry, and the horizontal portion of the Beam Find circuitry are also part of the Horizontal Amplifier circuitry. The Horizontal Preamplifiers amplify input signals for application to the Horizontal Output Amplifier.

X1/X5 Horizontal Preamplifier.

The X1/X5 amplifier is a differential stage consisting of Q747, Q748, and associated components. When the X5 MAG line is LO, the X1 gain is set by resistor network R775 and R753, with current supplied through Q750. When X5 MAG is selected (HI), Q750 is switched off, and current is supplied through R730. Potentiometer R730 is adjusted to balance the current through Q747 and Q748. The X5 gain is set by R753, R755, R731, and R749. When in X1 mode, CR747 and CR748 are reverse biased so that the X5 stage has no effect.

X1/X10 Horizontal Preamplifier

The X1/X10 amplifier is a cascode differential amplifier consisting of U745, U755, and associated components. Signals from the X1/X5 Preamplifier are buffered by emitter followers Q759 and Q760 before being applied to the bases of U745C and U745D. When the X10 MAG line is LO (X1 selected), U755B and U755E are biased off, and U755A and U745E are biased on. Diodes CR773 and CR774 are reverse biased. The gain will then be set by R763. When X10 MAG is HI, U755B, U755E, CR773, and CR774 are biased on, and U755A and U745E are biased off. The gain of the X10 stage is set by R763, R767, and R777. Potentiometer R782 balances the currents in the preamplifier so that there is no horizontal trace shift when switching between X1 and X10 modes. Capacitors C773 and C755 damp the high-frequency gain of the preamplifier.

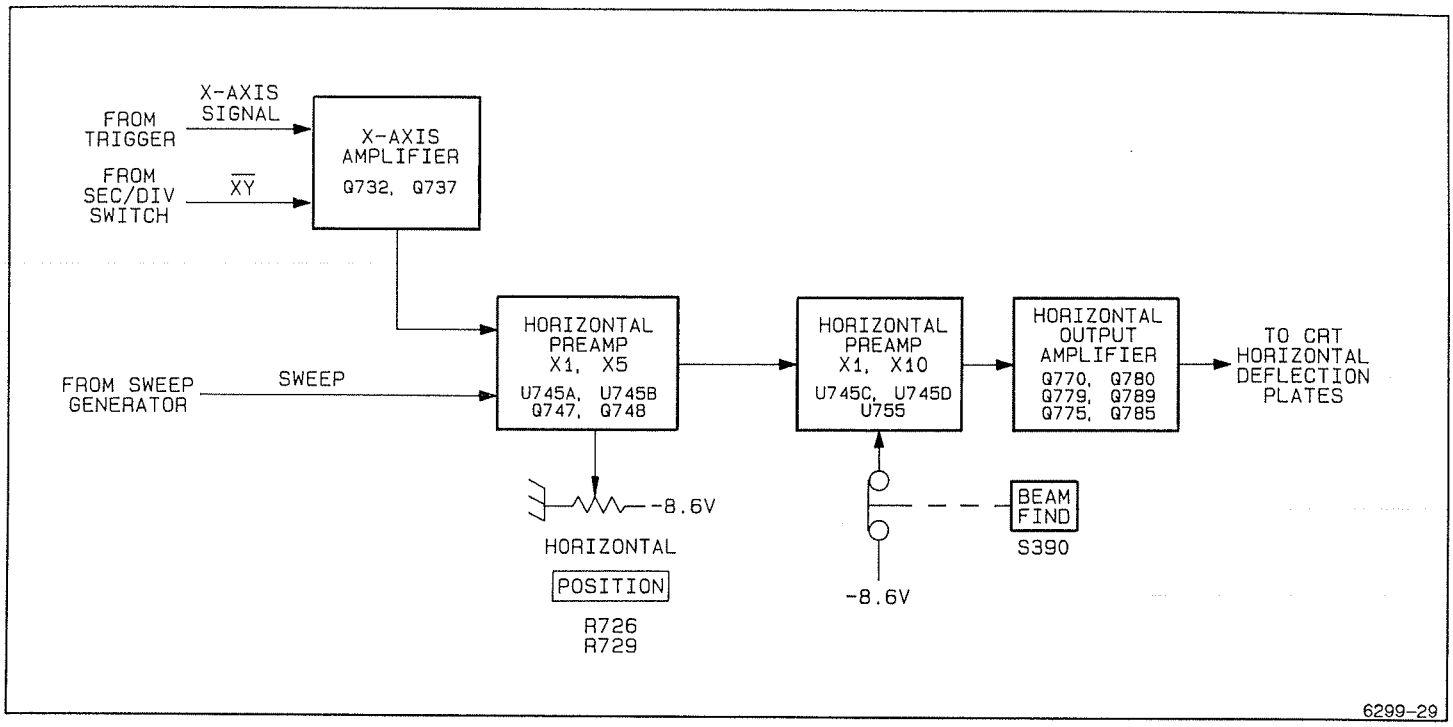

Figure 3-4. Block diagram of the Horizontal Amplifier circuit.

X-Y Amplifier

The X-Y Amplifier amplifies the Channel 1 signal (X-AXIS) from the Internal Trigger circuitry (diagram 3) and passes it to the Horizontal Preamplifier.

In the X-Y mode of operation, the $\overline{XY}$ line is pulled LO by a switch contact on S701 (the SEC/DIV switch). This LO biases Q732 on in the linear region. The circuit of Q732 and Q737 is a transconductance amplifier that changes an input voltage to output current. The input signal is applied through X-Gain adjust potentiometer R395 (diagram 3). The X-Axis Offset adjustment is R736. The signal current out of Q737 is fed into the shunt feedback stage consisting of U745A, U745B, R741, R742, R743, R744, and R745. Resistors R741 and R742 set the gain of the stage. The network consisting of R711, R712, R713, R714, and C714 improves the power supply noise rejection. The output of the shunt feedback stage drives the preamplifiers in all horizontal modes. The sweep is held at a constant low output level when in X-Y mode.

When in the sweep mode, the $\overline{XY}$ line is HI, and Q732 is biased off. This in turn biases Q737 off and disables the X-Y Amplifier.

The $\overline{XY}$ line also turns U380B on (see diagram 3), thereby not allowing the X-AXIS signal to get to the X-Y amplifier. The sweep signal is applied through gain setting resistor R740 to the shunt feedback stage. The output of the shunt feedback stage drives the X1/X5 Preamplifier.

Horizontal Output Amplifier

The Horizontal Output Amplifier provides final amplification of the horizontal signal to drive the horizontal crt deflection plates.

Signals from the (+) and (-) sweep outputs of U755 drive two shunt-feedback amplifiers. Due to the feedback, the input impedance of these amplifiers is low. The base voltages of Q770 and Q780 are biased at nearly the same dc level by the forward-biased diodes (CR781 and CR791) located between the two emitters.

Transistors Q770, Q775, and Q779 form a cascode-feedback amplifier for driving the right crt horizontal deflection plate. Amplifier gain is set by R784, with C784 providing high-frequency compensation. For low-speed signals, Q779 serves as a current source for Q775. At high sweep rates, the deflection signal is coupled through C785 to the emitter of Q779 to provide added pull-up output current to drive the

crt. The amplifier formed by Q780, Q785, and Q789 drives the left crt horizontal deflection plate in the same manner as described above, with zener diode VR792 shifting the collector signal level of Q780 to the correct level to drive the emitter Q785.

Horizontal Beam Find

The BEAM FIND switch is buffered by emitter follower Q776. Diodes CR780 and CR790 are normally reverse biased by R776 when BEAM FIND is off. When BEAM FIND is active, Q776 is turned on, and its emitter is driven negative to about -8 V. The voltage on the cathode of VR776 drops to about 5 V, causing CR780 and CR790 to be forward biased. Current through CR780 and CR790 cause the output common-mode voltage of the two shunt-feedback amplifiers to be shifted negative to reduce the available voltage swing at the crt plates. This stops the trace from being deflected off-screen horizontally.

FRONT PANEL

The Front Panel circuitry is shown in diagram 6. Many of the switches and potentiometers are also shown on the other schematic diagrams adjacent to the circuitry controlled. Diagram 6 provides a diagram of the complete Front Panel to aid in servicing that circuit board. The active circuitry on the Front Panel includes the External Trigger buffer Amplifier, Q370B and Q370A, and the Horizontal Position Control current source, Q725. Operation of the FET External Trigger Buffer Amplifier is similar to the Channel 1 and Channel 2 Source Followers described previously.

All mode switching for the Vertical, Horizontal, and Trigger circuitry is done by the Front Panel switches.

Z-AXIS AMPLIFIER

The Z-Axis Amplifier, shown on diagram 7, controls the crt intensity level via several input-signal sources. The effect of these input signals is either to increase or decrease trace intensity or to completely blank portions of the display. The Z-Axis signal current as determined by the Z-Axis switching logic and the input current from the EXT INPUT OR Z connector (if in use), are summed at the emitter of common-base amplifier Q825. The summed current thereby sets the collector current of the stage. The common-base amplifier provides a low-impedance termination for the input signals and isolates the signal sources from the rest of the Z-Axis Amplifier.

Common-base transistor Q829 passes a constant current through R832. This current is divided between Q825 and Q829, with the portion through Q829 driving the shunt-feedback output amplifier formed by Q835, Q840, and Q845. The bias level of Q825 therefore controls the emitter current available to Q829. Feedback-resistor R841 sets the transresistance gain for changing the input current to a proportional output voltage. Emitter-follower Q835 is dc coupled to Q840; and, for low-speed signals, Q845 acts as a current source. Fast transitions couple through C845, providing added current gain through Q845 for fast voltage swings at the output of the amplifier.

External Z-Axis input voltages establish proportional input currents through R823, and amplifier sensitivity is determined by the transresistance gain of the shunt-feedback amplifier. Diode CR823 protects the Z-Axis Amplifier if excessive signal levels are applied to the EXT INPUT OR Z connector.

The INTENSITY potentiometer controls the base voltage of Q804 to set the amount of emitter current that flows through that transistor and, therefore, the level of the Z-Axis signal.

When the sweep is displayed, the emitter of Q817 is LO, causing CR817 to be reverse biased. Diodes CR816, CR821, and CR820 are also reverse biased. This allows the current through R818 to flow through CR818 and turn on the Z-Axis.

When X-Y is displayed, CR817 and CR816 are forward biased, reverse biasing CR821 and CR818. Diode CR819 is reverse biased, allowing the intensity to be set by the current through R820 and CR820.

When ALT MAG is selected, diodes CR816, CR817, CR819, and CR822 are all reverse biased, allowing the intensity to be controlled by the current flowing through R818 and R821. This action therefore increases the intensity of the MAG trace.

When CHOP Vertical MODE is selected, the CHOP BLANK signal is sent to the collector of Q825 through CR824 during the display-switching time. Diode CR825 is reverse biased, and the forward bias of Q829 rises to the blanking level. When blanked, the output of the Z-Axis Amplifier drops to reduce the crt beam current below viewing intensity.

At high beam currents, the crt cathode voltage tends to drop off slightly. To compensate for this,

the 2-kV winding is referenced to the emitter of Q804, so that the output of the multiplier (12 kV) is reduced slightly at high intensity levels.

Z-Axis Beam Find

When the BEAM FIND button is pressed, the BEAM FIND line goes to about -8 V. This voltage level will shunt about 1 mA from the Z-Axis Amplifier, overriding any other current combinations to unblank the trace.

DC Restorer and Multiplier

The DC Restorer circuit sets the crt control-grid bias and couples the ac and dc components of the Z-Axis Amplifier output to the crt control grid. Direct coupling of the Z-Axis Amplifier output to the crt control grid is not employed due to the high potential differences involved. Refer to Figure 3-5 during the following discussion.

Ac drive to the DC Restorer circuit is obtained from pin 4 of T902. The drive voltage has an ac peak amplitude of about 100V, at a frequency of about 20 kHz and is coupled into the DC Restorer circuit through C853 and R853. The cathode of CR851 is biased by the wiper voltage of Grid Bias potentiometer R851, and the ac-drive voltage is clamped whenever the positive peaks reach a level that forward biases CR851.

The Z-Axis Amplifier output voltage, varying with display intensity between +10 V and +75 V, is applied to the DC Restorer at the anode of CR853. The ac-drive voltage holds CR853 reverse biased until the voltage falls below the Z-Axis Amplifier output voltage level. At that point, CR853 becomes forward biased and clamps the junction of CR851, CR853, and R854 to the Z-Axis output level. Thus, the ac-drive voltage is clamped at two levels to produce a square-wave signal with a positive dc-offset level.

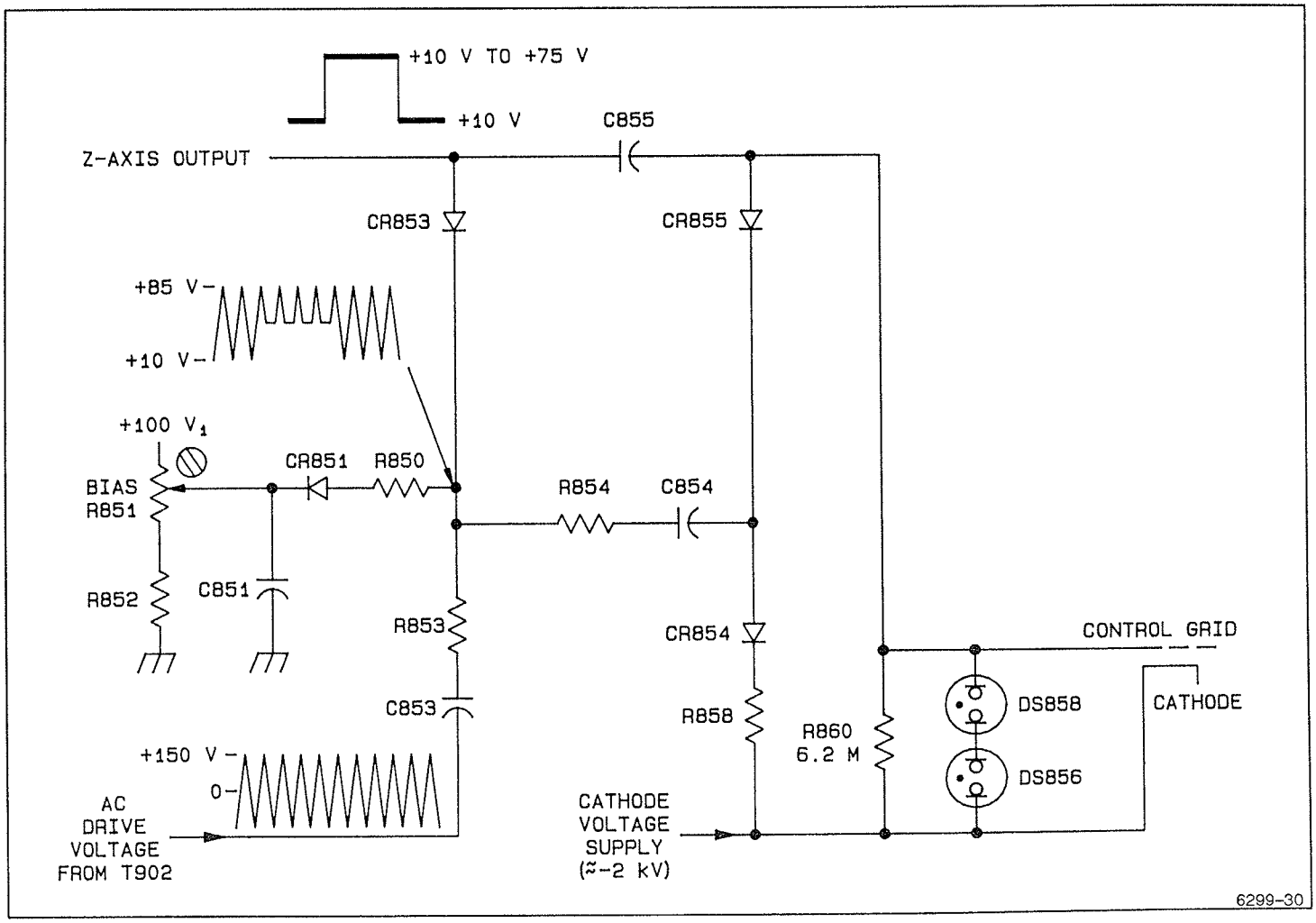

Figure 3-5. Simplified diagram of the DC Restorer circuitry.

The DC Restorer is referenced to the -2-kV crt cathode voltage through R858 and CR854. Initially, both C855 and C854 charge up to a level determined by the difference between the Z-Axis output voltage and the crt cathode voltage. Capacitor C855 charges from the Z-Axis output through R858, CR854, and CR855 to the crt cathode. Capacitor C854 charges through R858, CR854, R854, and CR853 to the crt cathode.

During the positive transitions of the ac drive, from the lower clamped level toward the higher clamped level, the charge on C854 increases due to the rising voltage. The voltage increase across C854 is equal to the amplitude of the positive transition. The negative transition is coupled through C854 to reverse bias CR854 and to forward bias CR855. The increased charge of C854 is then transferred to C855 as C854 discharges toward the Z-Axis output level. Successive cycles of the ac input to the DC Restorer charge C855 to a voltage equal to the initial level plus the amplitude of the clamped square-wave input.

The added charge held by C855 sets the control-grid bias voltage. If more charge is added to that already present on C855, the control grid becomes more negative, and less crt writing-beam current flows. Conversely, if less charge is added, the control-grid voltage level becomes closer to the cathode-voltage level, and more crt writing-beam current flows.

During periods that C854 is charging, the crt control-grid voltage is held constant by the long time-constant discharge path of C855 through R860.

Fast-rise and fast-fall transitions of the Z-Axis output signal are coupled to the crt control grid through C855 to start the crt writing-beam current toward the new intensity level. The DC Restorer output level then follows the Z-Axis output-voltage level to set the new bias voltage for the crt control grid.

Neon lamps DS858 and DS856 protect the crt from excessive grid-to-cathode voltage if the potential on either the control grid or the cathode is lost for any reason.

High-voltage multiplier U975 uses the 2-kV winding of T902 to generate 12 kV to drive the crt anode. An internal half-wave rectifier diode in the multiplier produces -2 kV for the crt cathode. The -2-kV supply is filtered by a low-pass filter formed by R975, C975, C976, R976, R978, and C979. Neon lamp DS870 protects against excessive voltage between the crt heater and crt cathode by conducting if the voltage difference exceeds approximately 75 V.

Focus voltage is also developed from the -2-kV supply by a voltage divider formed by R894, R892, FOCUS potentiometer R893, R891, R890, R889, R888, R886, and Q885. The focus voltage tracks the intensity level through the action of Q885. The emitter voltage of Q804, set by the INTENSITY control, is applied to the emitter of Q885 through R885. When the emitter voltage of Q804 changes, the current through Q885 changes proportionally and alters the voltage at one end of the FOCUS control.

POWER SUPPLY

The Power Supply circuitry (diagram 7) converts the ac-power-line voltage into all the voltages required by the instrument. It comprises the Mains Input Board, Transformer, Preregulator, Series Pass, and Inverter circuits.

Mains Input Board

The power switch (S901) connects the ac-power line to the primary winding of the toroidal wound input transformer, T901, via fuse F901, filter components L901, L902, C903, C904, C905, and VOLTS SELECTOR switch S902. The secondary output is rectified and smoothed by CR901, CR902, CR903, CR904 and C900. With an ac-input voltage of 240 V, there is approximately 60 V between W903-pin 1 and W903-pin 2 at full load.

LINE SYNC. The additional components on the Mains Input Board produce a Line Sync signal for the Trigger circuit. Transistor Q900 is a floating differential amplifier with a dc bias network comprising R905, R904, and R902. Resistors R906 and R903 apply a small line-frequency signal from the secondary of T901 to the base-emitter junction of Q900. The resultant collector current of Q900 is a line-frequency, sine-wave signal that is fed via W903-3 to the Main board.

Preregulator

The 60-V power supply from the Mains Input board, is applied to the Preregulator circuit formed by U910, Q913, and associated components. Zener diode VR910 and R910 reduce the incoming supply

for preregulator U910. The Preregulator oscillates at a nominal 39 kHz, as determined by timing components C908 and R908. The square-wave output is level-shifted by Q911, and fed to the Darlington pair circuit formed by Q912 and power transistor Q913. When Q913 is conducting, current ramps up through L910. When Q913 is off, the current ramps down while flowing in through the flywheel diode CR912. Preregulator U910 varies the duty cycle of conduction of Q913, so that the voltage on filter capacitor C914 is a nominal 39.5 V. The network R917, R922, R932, R934, and CR915 monitors the voltage across Q923; and, if that voltage is lower than the nominal 1.4 V, U910 increases the voltage across C914 until Q923 has the correct voltage.

If Q923 is open circuited, CR915 clamps the lower supply voltage to 31 V. The ratio of R932 and R922 across R934 together with R917, is chosen so that if Q923 is short circuited, the maximum voltage across C914 is 41 V. Thus the Preregulator supplies a sensible output under all conditions of the circuitry which it drives except during an overload condition. In this case the voltage developed across the current sense resistor (R907) reaches the offset voltage of 180 mV developed by R910 and R911, and U910 current limits the output to about 900 mA.

Series Pass

The function of Series Pass transistor Q923, is to reject ripple current having a frequency of twice the power-line frequency. The nominal DC voltage across it is only 1.4 V. Base current is supplied to Q923 via R923 and CR923 in the absence of drive from Q921, when the instrument is first switched on. Transistor Q923 is driven by both halves of U920 through Q921. The output at pin 7 of U920 serves to reject hum on the 38-V supply by comparing the output of potential divider R930 and R929, with the reference diode VR931. The output at pin 1 of U920, slightly varies the value of the reference as seen at pin 6 via attenuator resistors R925 and R926. This variation maintains the -8.6-V supply at the value set by the -8.6-V Set potentiometer, R933.

Inverter

Inverter oscillator U940 is driven via Q918 and R946, at the same frequency as U910. U940 supplies two non-overlapping complimentary square-wave outputs to Q930 and Q960. These transistors are in feedback loops, one of which is formed by the filter R953, CR953, reservoir capacitor C953, and level shifter VR939. The feedback is such that the base of Q940 is adjusted to drive Q950 sufficiently hard that the emitter swings to within 3 V of ground, but not hard enough to saturate it. The output voltages of transformer T902 secondary windings are full-wave rectified. The 100-V supply voltage is derived from an auto-transformer winding in series with the primary winding. Resistors R942 and R941 feed a sample of the 38-V supply voltage into the error amplifier connected to pins 1 and 2 of U940. If the 38-V supply should go high, U940 will shut down.

Probe Adjust

The Probe Adjust circuitry, shown on diagram 4, is a square-wave generator and diode switching network that produces a negative-going, square-wave signal at the PROBE ADJUST terminal, J590. Amplifier U580A forms a multivibrator that has an oscillation period set by the time constant of R587 and C587. When the output of the multivibrator is at the positive supply voltage, CR588 is forward biased. This reverse biases CR589, and the PROBE ADJUST signal is held at ground potential by R590. When the multivibrator output switches states, and is at the negative supply voltage level, CR588 is reverse biased. Diode CR589 becomes forward biased, and the circuit output level drops to approximately -0.5 V.

Power Distribution

Power routing from the power supply to the other circuit board is shown in diagram 8. The schematic shows jumpers that may be used to isolate suspected loads from the power supply when troubleshooting power supply problems.

Circuit Board Interconnections

The signal interconnections between circuit boards are shown in diagram 9. This diagram may be used as an aid in signal tracing between the boards. The connectors are also convenient locations to check for the signals between boards when troubleshooting.